What is Claimed is:

1. Dynamically adjustable differential output driver circuitry on an integrated circuit that transmits differential output data signals that have a peak-to-peak output voltage swing V_{OD}, comprising:

adjustable current source circuitry;

adjustable resistor circuitry;

switching circuitry for switching current from the adjustable current source circuitry through the adjustable resistor circuitry to produce the differential output signals, wherein the adjustable current source circuitry and adjustable resistor circuitry are controlled independently in real time by control signals to adjust the peak-to-peak output voltage swing V_{OD} of the differential output data signals.

2. The dynamically adjustable differential output driver circuitry defined in claim 1 further comprising an adjustable voltage source, wherein the differential output data signals have a common-mode voltage V_{CM} that is controlled by adjusting the adjustable voltage source.

3. The dynamically adjustable differential output driver circuitry defined in claim 1 further comprising dynamic control circuitry that generates the control signals that control the adjustable current source circuitry and the adjustable resistor circuitry.

4. The dynamically adjustable differential

output driver circuitry defined in claim 1 further comprising dynamic control circuitry that generates control signals that control the adjustable voltage source.

5. The dynamically adjustable differential output driver circuitry defined in claim 1 further comprising dynamic control circuitry that generates the control signals, wherein the dynamic control circuitry is implemented at least partly using programmable logic circuitry.

6. Dynamically adjustable differential output driver circuitry on an integrated circuit that transmits differential output data signals that have a common-mode voltage V_{CM}, comprising:

current source circuitry;

resistor circuitry;

switching circuitry for switching current from the current source through the resistor circuitry to produce the differential output signals;

an adjustable voltage source that applies a voltage to the resistor circuitry that establishes the common-mode voltage V_{CM} for the differential output data signals; and

dynamic control circuitry responsive to feedback signals from another integrated circuit, wherein the dynamic control circuitry adjusts the voltage applied to the resistor circuitry by the adjustable voltage source based on the feedback signals to adjust the common-mode voltage V_{CM}.

7. The dynamically adjustable differential output driver circuitry defined in claim 6 wherein the current source circuitry comprises adjustable current source circuitry.

8. The dynamically adjustable differential output driver circuitry defined in claim 6 wherein the resistor circuitry comprises process and temperature compensation circuitry to compensate for process-induced and temperature-induced resistivity changes in the resistor circuitry.

9. The dynamically adjustable differential output driver circuitry defined in claim 6 further comprising programmable circuitry, wherein the differential output data signals have a peak-to-peak output voltage swing V_{OD}, wherein the resistor circuitry comprises adjustable resistor circuitry, wherein the current source circuitry comprises adjustable current source circuitry, and wherein the adjustable resistor circuitry and the adjustable current source circuitry are independently adjustable to adjust the peak-to-peak output voltage swing V_{OD}.

10. The integrated circuit defined in claim 6 wherein the other integrated circuit has a differential input driver with an associated common-mode voltage level, wherein the differential input driver receives the differential output data signals from the integrated circuit, and wherein the dynamic control circuitry

adjusts the adjustable voltage source based on the feedback signals to match the common-mode voltage V_{CM} of the differential output data signals to the common-mode voltage level of the differential input driver on the other integrated circuit.

11. An integrated circuit, comprising:

a dynamically adjustable differential output driver that produces differential output data signals having a peak-to-peak output voltage swing V_{OD}; and

dynamic control circuitry that receives information from another integrated circuit to which the differential output data signals are transmitted and which controls the dynamically adjustable differential output driver dynamically in real time to adjust the peak-to-peak output voltage swing V_{OD} based at least partly on the information received from the other integrated circuit.

12. The integrated circuit defined in claim 11 further comprising programmable core logic, wherein at least part of the dynamic control circuitry is implemented in the programmable core logic.

13. The integrated circuit defined in claim 11 wherein the dynamically adjustable differential output driver comprises adjustable current source circuitry and wherein the dynamic control circuitry adjusts the peak-to-peak output voltage swing V_{OD} by adjusting the adjustable current source circuitry.

14. The integrated circuit defined in claim 11 wherein the dynamically adjustable differential output driver comprises adjustable resistor circuitry and wherein the dynamic control circuitry adjusts the peak-to-peak output voltage swing V_{OD} by adjusting the adjustable resistor circuitry.

15. The integrated circuit defined in claim 11 wherein:

the dynamically adjustable differential output driver comprises adjustable current source circuitry;

the dynamic control circuitry adjusts the peak-to-peak output voltage swing V_{OD} by adjusting the adjustable current source circuitry;

the dynamically adjustable differential output driver comprises adjustable resistor circuitry;

the dynamic control circuitry adjusts the peak-to-peak output voltage swing V_{OD} by adjusting the adjustable resistor circuitry; and

the dynamic control circuitry adjusts the adjustable current source circuitry independently from the adjustable resistor circuitry.

16. The integrated circuit defined in claim 11 wherein the differential output data signals have a common-mode voltage V_{CM} and wherein the dynamically adjustable differential output driver comprises an adjustable voltage source that the dynamic control circuitry adjusts based at least partly on the

information received from the other integrated circuit to control the common-mode voltage V_{CM} of the differential output data signals.

17. The integrated circuit defined in claim 11 wherein the differential output data signals have a common-mode voltage, wherein the information received from the other integrated circuit comprises feedback signals associated with the differential output data signals as received at the other integrated circuit, and wherein the dynamically adjustable differential output driver comprises an adjustable voltage source that the dynamic control circuitry adjusts to control the common-mode voltage of the differential output data signals based on the feedback signals.

18. The integrated circuit defined in claim 11 wherein the differential output data signals have a common-mode voltage when transmitted from the integrated circuit to a differential input driver on the other integrated circuit, wherein the differential input driver has a common-mode voltage level, wherein the information received from the other integrated circuit comprises information on the common-mode voltage level of the differential input driver, and wherein the dynamically adjustable differential output driver comprises an adjustable voltage source that the dynamic control circuitry adjusts to match the common-mode voltage of the differential output data signals to the common-mode voltage level of the differential input driver.

19. A system comprising:

a first integrated circuit having:

a dynamically adjustable differential output driver that produces differential output data signals having a common mode voltage V_{CM} and a peak-to-peak output voltage swing V_{OD}; and

dynamic control circuitry that that controls the dynamically adjustable differential output driver;

a communications path to which the differential output data signals are provided by the differential output driver; and

a second integrated circuit having:

a differential input driver that receives the differential output data signals from first integrated circuit over the communications path; and

monitoring and feedback circuitry that provides feedback information to the first integrated circuit that is based on the received differential output data signals from the first integrated circuit, wherein the dynamic control circuitry on the first integrated circuit controls the dynamically adjustable differential output driver in real time based on the feedback information received from the monitoring and feedback circuitry on the second integrated circuit.

20. The system defined in claim 19 wherein the first integrated circuit comprises a programmable logic device comprising programmable core logic.

21. The system defined in claim 19 wherein the first integrated circuit comprises a programmable logic device having programmable core logic in which at least part of the dynamic control circuitry is implemented.

22. The system defined in claim 19 wherein the dynamically adjustable differential output driver includes adjustable programmable resistor circuitry and programmable current source circuitry that are independently adjusted to set the peak-to-peak output voltage swing V_{OD} of the differential output data signals.

23. The system defined in claim 19 wherein the monitoring and feedback circuitry determines how much noise is present in the data signals at the input driver and provides the feedback information to the first integrated circuit at least partially based on the amount of measured noise.

24. The system defined in claim 19, wherein the differential input driver has an associated common-mode voltage level and wherein the dynamic control circuitry uses the feedback information to adjust the dynamically adjustable differential output driver to match the common-mode voltage of the differential output data signals to the common-mode voltage level of the differential input driver.

25. The system defined in claim 19 wherein the differential output driver and differential input driver form a first differential data channel and wherein there are a plurality of such differential data channels between the first integrated circuit and at least one other integrated circuit, each channel having its own associated level of peak-to-peak output voltage swing V_{OD} for its associated differential output data signals, wherein the dynamic control circuitry independently adjusts the differential output driver in each channel to adjust the level of the peak-to-peak output voltage swing V_{OD} for each channel.

26. The system defined in claim 19 wherein the differential output driver and differential input driver form a first differential data channel and wherein there are a plurality of such differential data channels between the first integrated circuit and at least one other integrated circuit, each channel having its own associated common-mode voltage V_{CM} for its associated differential output data signals, wherein the dynamic control circuitry independently adjusts the differential output driver in each channel to adjust the common-mode voltage V_{CM} for each channel.

27. A method for controlling a differential output driver that produces differential data signals that are transmitted between a first integrated circuit and a second integrated circuit over a differential communications path, comprising:

at the first integrated circuit, using

the differential output driver to transmit the differential data signals to the second integrated circuit over the communications path;

at the second integrated circuit, receiving the differential data signals transmitted from the first integrated circuit;

at the second integrated circuit, sending information to the first integrated circuit; and

at the first integrated circuit, receiving the information from the second integrated circuit and adjusting the differential output driver based on the received information.

28. The method defined in claim 27 wherein the information sent to the first integrated circuit comprises feedback signals that are produced at the second integrated circuit based on the received differential data signals from the first integrated circuit, the method further comprising:

at the first integrated circuit, adjusting the differential output driver based on the feedback signals.

29. The method defined in claim 27 wherein the differential data signals have a common-mode voltage and wherein the second integrated circuit receives the differential data signals using a differential input driver having an associated common-mode voltage level, the method further comprising:

at the first integrated circuit, using the information received from the second integrated

circuit to adjust the differential output driver so that the common-mode voltage of the differential data signals matches the common-mode voltage level associated with the differential input driver.

30. The method defined in claim 27 wherein there are a plurality of data channels associated with the first integrated circuit, each of which has a different associated differential output driver that produces differential data signals with an independent associated common-mode voltage V_{CM}, the method further comprising:

at the first integrated circuit, using the dynamic control circuitry to adjust the common-mode voltage V_{CM} of each channel independently.

31. The method defined in claim 27 wherein there are a plurality of data channels associated with the first integrated circuit, each of which has a different associated differential output driver that produces differential data signals with an independent associated peak-to-peak output voltage swing V_{OD}, the method further comprising:

at the first integrated circuit, using the dynamic control circuitry to adjust the peak-to-peak output voltage swing V_{OD} of each channel independently.

32. The method defined in claim 27 wherein the first integrated circuit comprise a programmable logic device, the method comprising at the first integrated circuit, adjusting the differential output

driver to adjust the differential output data signals without reprogramming the programmable logic device.